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EXAMINER	
NGUYEN, LINH M	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 08/25/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/600,120	Applicant(s) CHANG, RICHARD	
	Examiner Linh M. Nguyen	Art Unit 2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 June 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-33* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,6-8,12-15,20-22,24,28,29 and 32* is/are rejected.

7)☒ Claim(s) *5,9-11,16-19,23,25-27,30,31 and 33* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 June 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *10/14/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claims 1-33 are presented in the instant application according to the Applicants' filing on 06/20/2003.

Claim Objections/Minor Informalities

1. Claims 2, 12, 17 and 33 are objected to because of the following informalities:

Claim 2, line 4, end of line, insert "." after "number".

Claim 12, line 7, the term " phase shift selection circuit" has already been included in the preamble to denote the entire circuit, the term " phase shift selection circuit" used here, in line 7 of claim 12, is believed to point to component [411] of Fig. 4, as indicated at page 8 line 13 of the specification. It is suggested to change the term " phase shift selection circuit" used here, in line 7, to -- the phase shift circuit-- to a) avoid confusion for using the same term for two different units and b) to be consistent with the disclosure.

Claim 17, line 5, changing "a" (at end of line) to --the-- is suggested since antecedent basis has already been recited in line 3.

Claim 33, line 5, changing "a" to --the-- is suggested since antecedent basis has already been recited in line 3.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who

has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

3. Claims 1, 3, 4, 6, 7, 12, 20 and 28 are rejected under 35 U.S.C. 102(e) as being anticipated by Nguyen (U.S. Patent No. 6,600,355).

With respect to claim 1, Nguyen discloses, in Figure 12, a circuit arrangement and its corresponding method for changing a phase of a clock signal, the method comprising a) generating [1237] N clock signals that each has a period, wherein each of the N clock signals has the same period and a different phase; b) selecting first [1203] and second [1223] ones of the N clock signals to provide a selected clock signal and a phase forward clock signal using selection circuits; and in response to a phase change signal [RESET], shifting the phase of the selected clock signal and the phase forward clock signal by causing the selection circuit to select different ones of the N clock signals.

With respect to claim 3, Nguyen discloses, in Figure 12, a step of shifting the phase of the selected clock signal by 360°/N in response to a phase change signal further comprises shifting phases of the selected clock signal and the phase forward clock signal backward by 360°/N on an edge of the selected clock signal, and shifting the phases of the selected clock signal and the phase forward clock signal forward by 360°/N on an edge of the phase forward clock signal, as

called for in claim 3 *(forward shifting and backward shifting of both the selected clock signal and the phase forward clock signal are dependent on the select signals (S270,S180,S90,S0)).*

With respect to claim 4, Nguyen discloses, in Figure 12, a step of shifting the phases of the selected clock signal and the phase forward clock signal further comprises changing values of first and second select signals in response to the phase change signal [RESET]; selecting a different one of the N clock signals to shift the phase of the selected clock signal in response to the changed value of the first select signal; and selecting a different one of the N clock signals shift the phase of the phase forward clock signal in response to the changed value of the second select signal.

With respect to claim 6, Nguyen discloses, in Figure 12, that binary value of the first and the second select signals are shifted in one direction to increase the phases of the selected clock signal and the phase forward clock signal by 360°/N, and the binary values of the first and the second select signals are shifted in a second direction to decrease the phases of the selected clock signal and the phase forward clock signal by 360°/N *(forward shifting and backward shifting of both the selected clock signal and the phase forward clock signal are dependent on the select signals (S270, S180, S90, S0))*.

With respect to claim 7, Nguyen discloses, in Figure 12, a circuit arrangement and a corresponding method for changing a phase of an output clock signal, the method comprising a) providing first and second clock signals [1237] having different phases, in response to a phase change signal [RESET], shifting the phases of the first and the second clock signals backward on an edge of the first clock signal; in response to the phase change signal [RESET], shifting the

phases of the first and the second clock signals forward on an edge of the second clock signal; and providing the first clock signal as the output signal.

With respect to claim 12, Nguyen discloses, in Figure 12, a phase shift selection circuit comprising a) a first multiplexer [1203] that selects one of N clock signals that have different phases to provide an output clock signal; b) a second multiplexer that selects one of the N clock signals to provide a phase foward signal, a phase of the output clock signal being offset from a phase of the phase forward signal by 360°/N *(depending on the selection signals [R0, R90, R180, R270] and [S0, S90, S180,S270]*; and c) a phase shift selection circuit [1237,1201, 1221] that dynamically shifts the phases of the output clock signal and the phase forward signal by 360°/N in response to a phase change signal by causing the first and the second multiplexers to select different ones of the N clock signals.

With respect to claim 20, Nguyen discloses, in Figure 12, a phase shift selection circuit comprising a) a first multiplexer [1203] that selects one of a plurality of clock signals to provide an output clock signal, each of the clock signals having a different phase; b) a second multiplexer that selects one of the clock signals to provide a phase forward clock signal; and c) a multiplexer control circuit [1201,1221,RESET] that decreases phases of the output and the phase forward clock signals on an edge of the output clock signal, and increases the phases of the output and the phase forward clock signals on an edge of the phase forward clock signal in response to a phase change signal.

With respect to claim 28, Nguyen discloses, in Figure 12, a method for changing a phase of a clock signal, the method comprising a) generating [1237] N clock signals that each have a

period, wherein each of the N clock signals has the same period and a different phase; b) selecting [1203] a first one of the N clock signals to provide a selected clock signal using a Multiplexer circuit [1203]; c) changing a voltage of a phase change signal [RESET] while the multiplexer circuit is ON; and d) in response to the changed voltage of the phase change signal, shifting *(depending on the select signals [S0, S90, S180, S270])* the phase of the selected clock signal by causing the multiplexer to select a different one of the N clock signals, wherein shifting the phase of the selecting clock signal does not cause glitches in the selected clock signal.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 2, 15 and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nguyen (U.S. Patent No. 6,600,355), in view of Larsson (U.S. Patent No. 6,157,694).

With respect to claims 2, 15 and 24, Nguyen discloses all of the claimed limitations as expressly recited in claims 1, 12 and 20, except for the step of dividing the frequency of the selected clock signal by a fractional value to generate an output clock signal, a frequency of the output clock signal being 1/M times the frequency of one of the N clock signals, wherein M is not a whole number.

Larsson discloses, in Fig. 1, a counter [16] for dividing an output signal of a multiplier [12] by a fraction to make a transition from low to high completing one full output clock.

To configure the circuit of Nguyen with a counter coupled to the selected clock signal by a fraction value to generate an output clock signal as taught by Larsson so that the produced output signals would have a high degree of symmetry relative to each other rendering the these output signals suitable for use in systems requiring little jitter would have been obvious to one of ordinary skill in the art at the time of the invention since Larsson teaches that such configuration would facilitate a high degree of symmetry *(see Larsson, col.17, lines 39-42).*

6. Claims 8, 13, 14, 20-22, 29 and 32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nguyen (U.S. Patent No. 6,600,355), in view of Rieven (U.S. Patent No. 6,580,304).

With respect to claims 8, 13 and 21, Nguyen discloses all of the claimed limitations as expressly recited in claim 7, 12 and 20, and (from claim 8) generating [1237] N clock signals and phases of the N clock signals being separated by 360°/N, and a period of each of the N clock signals having the same length, wherein the first clock signal [S] is selected from among the N clock signals using a first multiplexer [1203], and the second clock signal is selected from among the N clock signals using a second multiplexer [1223].

Nguyen discloses, in Fig. 12, that the step of generating N clock signals being performed by DLL (Delay Locked Loop) [1237] but fails to provide the details of the DLL circuit, which includes an oscillator.

Rieven discloses, in Figs. 4 and 4A, a DLL circuit including an oscillation circuitry [Fig. 4A, item 125] and delay chains [118, 122, 130, 132] for generating clock signals.

To configure the circuit of Nguyen with a circuit for generating a plurality (N) clock signals having oscillation circuitry as taught by Rieven for high precision delays would have been obvious to one of ordinary skill in the art at the time of the invention since Rieven teaches that such configuration would provide precision delays and compensating for nonuniformity in the precision delay *(see Rieven, col. 3, lines 63-65).*

With respect to claims 14 and 22, Nguyen discloses all of the claimed limitations as expressly recited in claims 12 and 20. Nguyen discloses, in Fig. 12, that the phase shift selection circuit includes a DLL (Delay Locked Loop) [1237] connected to the first [1203] and second [1223] multiplexers for generating N clock signals but fails to provide the details of the DLL circuit, which includes adjustable delay circuits.

Rieven discloses, in Figs. 4 and 4A, a DLL circuit including delay chains [118, 122, 130, 132] for generating clock signals.

To configure the circuit of Nguyen with a circuit for generating a plurality (N) clock signals having the adjustable delay circuit as taught by Rieven for high precision delays would have been obvious to one of ordinary skill in the art at the time of the invention since Rieven teaches that such configuration would provide precision delays and compensating for nonuniformity in the precision delay *(see Rieven, col. 3, lines 63-65).*

With respect to claim 29, Nguyen discloses, in Figure 12, a phase shift selection circuit comprising a) a first multiplexer [1203] that selects one of N clock signals that have different phases to provide an output clock signal; b) a second multiplexer that selects one of the N clock

signals to provide a phase foward signal, a phase of the output clock signal being offset from a phase of the phase forward signal by 360°/N *(depending on the selection signals [R0, R90, R180, R270] and [S0, S90, S180,S270]*; and c) a phase shift selection circuit [1237,1201, 1221] that dynamically shifts the phases of the output clock signal and the phase forward signal by 360°/N in response to a phase change signal by causing the first and the second multiplexers to select different ones of the N clock signals.

Nguyen discloses, in Fig. 12, a DLL for generating a plurality of clock signal having different phases but fails to disclose details of DLL, which includes a delay circuit that generates N clock signals that have different phases.

Rieven discloses, in Figs. 4 and 4A, a DLL circuit including delay chains [118, 122, 130, 132] for generating clock signals signal having different phases.

To configure the circuit of Nguyen with a circuit for generating a plurality (N) clock signals having the adjustable delay circuit as taught by Rieven for high precision delays would have been obvious to one of ordinary skill in the art at the time of the invention since Rieven teaches that such configuration would provide precision delays and compensating for nonuniformity in the precision delay *(see Rieven, col. 3, lines 63-65).*

With respect to claim 32, Nguyen discloses, in Figure 12, a phase shift selection circuit comprising a) a first multiplexer [1203] that selects one of N clock signals that have different phases to provide an output clock signal; b) a second multiplexer that selects one of the N clock signals to provide a phase foward signal, a phase of the output clock signal being offset from a phase of the phase forward signal by 360°/N *(depending on the selection signals [R0, R90, R180, R270] and [S0, S90, S180,S270]*; and c) a phase shift selection circuit [1237,1201, 1221] that

dynamically shifts the phases of the output clock signal and the phase forward signal by 360°/N in response to a phase change signal by causing the first and the second multiplexers to select different ones of the N clock signals.

Nguyen discloses, in Fig. 12, that the step of generating N clock signals being performed by DLL (Delay Locked Loop) [1237] but fails to provide the details of the DLL circuit, which includes an oscillator.

Rieven discloses, in Figs. 4 and 4A, a DLL circuit including an oscillation circuitry [Fig. 4A, item 125] and delay chains [118, 122, 130, 132] for generating clock signals.

To configure the circuit of Nguyen with a circuit for generating a plurality (N) clock signals having oscillation circuitry as taught by Rieven for high precision delays would have been obvious to one of ordinary skill in the art at the time of the invention since Rieven teaches that such configuration would provide precision delays and compensating for nonuniformity in the precision delay *(see Rieven, col. 3, lines 63-65).*

Allowable Subject Matter

7. Claims 5 and 9-11, 16-19, 23, 25-27, 30, 31 and 33 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

8. The following is a statement of reasons for the indication of allowable subject matter:

The closest prior art on record does not show or fairly suggest:

a) The method, in which the first and the second select signals are count signals, the phase of the selected clock signal and the phase forward clock signal shifting forward by 360°/N

when the first and the second select signals increase, the phase of the selected clock signal and the phase forward clock signal shifting backward by 360°/N when the first and the second select signals decrease, as called for in claim 5;

b) The method, in which the phases of the first and the second clock signals are shifted backward when a directional signal is a first value, and the phases of the first and the second clock signals are shifted forward when the directional signal is a second value, as called for in claim 9;

c) The phase shift selection circuit further comprising a third multiplexer that selectively couples the output clock signal and the phase forward signal to an input of the phase selection circuit, as called for in claim 16;

d) The phase shift selection circuit, in which the phase shift (selection) circuit increases the phases of the output clock signal and the phase forward signal by 360°/N on an edge of the phase forward signal when a directional signal is a first value, and the phase shift selection circuit decreases the phases of the output clock signal and the phase forward signal by 360°/N on an edge of the output clock signal when the directional signal is a second value, as called for in claim 17;

e) The phase shift selection circuit, in which the phase shift selection circuit is a counter circuit that generates first and second count signals that control the first and the second multiplexers, respectively, values of the first and the second count signals changing in response to the phase change signal, as called for in claims 18 and 30;

f) The phase shift selection circuit, in which the phase shift (selection) circuit is a cyclic shift register that generates a first set and second set of digital signals that control the first and

the second multiplexers, respectively, values of the first and the second sets of digital signals shifting in response to the phase change signal, as called for in claims 19, 25 and 31;

g) The phase shift selection circuit, in which the multiplexer control circuit is a counter circuit that generates a first count signal at the first output and a second count signal at the second output, the first and the second count signals changing in response to the phase change signal, as called for in claim 23;

h) The phase shift selection circuit, in which a third multiplexer coupled to receive the output clock signal and the phase forward clock signal from the first and the second multiplexers, the third multiplexer having an output coupled to an input of the multiplexer selection circuit, as called for in claim 26;

i) The phase shift selection circuit, in which the multiplexer control circuit decreases the phases of the output and the phase forward clock signals when a phase direction signal is a first value, and the multiplexer control circuit increases the phases of the output and the phase forward clock signals when the phase direction signal is a second value, as called for in claim 27; and

g) The phase locked loop circuit, in which the phase shift selection circuit increases the phases of the output clock signal and the phase forward signal by 360°/N on an edge of the phase forward signal, when a directional signal is a first value, and the phase shift selection circuit decreases the phases of the output clock signal and the phase forward signal of 360°/N on an edge of the output clock signal when a directional signal is a second value, as called for in claim 33.

Citation of Relevant Prior Art

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Prior art Foley et al. (U.S. Pub. No. 2003/0234669) discloses methods and apparatus for synthesizing a clock signal.

Prior art Maggio et al. (U.S. Pub. No. 2002/0126785) discloses a method for recovering a clock signal in a telecommunications system and circuit thereof.

Inquiry

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Linh M. Nguyen whose telephone number is (571) 272-1749. The examiner can normally be reached on Alternate Fri, Monday - Thursday from 7:00 to 4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy P. Callahan can be reached on (571) 272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

LMN

LINH MY NGUYEN
PRIMARY EXAMINER